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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.          | CONFIRMATION NO.       |
|--|-------------|----------------------|------------------------------|------------------------|
| 10/059,488   | 01/28/2002  | Satoshi Shigematsu   | 96790p382                    | 5883                   |
| 8791 7590 10/18/2007<br>BLAKELY SOKOLOFF TAYLOR & ZAFMAN<br>1279 OAKMEAD PARKWAY<br>SUNNYVALE, CA 94085-4040 |             |                      | EXAMINER<br>JERABEK, KELLY L |                        |
|  |             |                      | ART UNIT<br>2622             | PAPER NUMBER           |
|  |             |                      | MAIL DATE<br>10/18/2007      | DELIVERY MODE<br>PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/059,488

**Applicant(s)**

SHIGEMATSU ET AL.

**Examiner**

Kelly L. Jerabek

**Art Unit**

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 5-10, 12-16, 19 and 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 11, 17 and 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/4/2007 has been entered.

### ***New Examiner of Record***

The prosecution of this application has been transferred to Examiner Kelly Jerabek from the docket of Examiner Gary Vieaux. Any inquiry concerning this Office Action or earlier communications should be directed to the current Examiner of record. Current contact information is provided in the last section of this communication.

### ***Response to Arguments***

Applicant's arguments filed 9/4/2007 have been fully considered but they are not persuasive.

**Response to Remarks:**

Applicant's arguments regarding claims 1 and 17 (Amendment pages 8-10) state that the Hou reference fails to disclose a counter for sequentially outputting count values in accordance with internal count operation and for operating independently of the matrix, and a maximum value of the counter being arbitrarily adjustable. The Examiner respectfully disagrees. Hou discloses a data conversion/output apparatus that includes a counter (311) which counts a clock signal (320) (col. 6, lines 45-58). The clock signal (320) is applied at mark time signal connector (310) from which the counter (311) counts the time marks in the clock signal (320) (col. 6, lines 47-50). Additionally, Hou states that the counter 311 continues counting of time marks and is reset only at the end of light integration (col. 6, lines 62-65). Thus, it can be seen that the counter operates independently of a pixel array, and a maximum value of the counter is arbitrarily adjustable (the counter 311 maximum value depends on the length of light integration). The Examiner notes that the claim language defining the counter is broad in scope and the Examiner is maintaining the rejection based on the broadest reasonable interpretation of the claim language. For example, the claim discloses that the counter operates independently of a pixel array. However, the claim does not mention that the counter operates independently of the plurality of sensors claimed.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claim 1-4 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Hou (US 6,578,145.)**

Re claim 1, Hou discloses a data conversion/output apparatus comprising a plurality of sensors (fig. 3, 302-1 – 302-n), voltage-time conversion circuits (fig. 3, 312-1 – 312-n) which are arranged adjacent to said respective sensors (fig. 3 302-1 – 302-n) and change output levels upon the lapse of times corresponding to output voltage values from said sensors after a conversion operation start point in order to convert voltage outputs of said sensors into times (col. 6 lines 41-44), and sensed data generation circuits (fig. 3, 314-1 – 314-n) for outputting, as digital data, lapse times until the output levels of said voltage-time conversion circuits change after a conversion start point (col. 6 lines 45-58), said sensed data generation circuits (fig. 3, 314-1 – 314-n) include a counter (311) for counting a clock signal (320) (col. 6, lines 45-58). The clock

signal (320) is applied at mark time signal connector (310) from which the counter (311) counts the time marks in the clock signal (320) (col. 6, lines 47-50). Additionally, Hou states that the counter 311 continues counting of time marks and is reset only at the end of light integration (col. 6, lines 62-65). Thus, it can be seen that the counter operates independently of a pixel array, and a maximum value of the counter is arbitrarily adjustable (the counter 311 maximum value depends on the length of light integration). The Examiner notes that the claim language defining the counter is broad in scope and the Examiner is maintaining the rejection based on the broadest reasonable interpretation of the claim language.

Re claim 2, Hou discloses all of the limitations of claim 2 (see the 102(e) rejection to claim 1 supra), including disclosing a data conversion/output apparatus further comprising control means for sequentially supplying outputs from said voltage-time conversion circuits to said sensed data generation circuits (col. 5 lines 30-44.)

Re claim 3, Hou discloses all of the limitations of claim 4 (see the 102(e) rejection to claim 1 supra), including wherein said sensors are arranged in a matrix together with said corresponding voltage-time conversion circuits to constitute respective pixels (fig. 3, in which indicator 302 and indicator 312 can be interpreted as one unit), and said data conversion/output apparatus further comprises group selection means for selecting, from the pixels in a column direction, pixels which are aligned in a row

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direction and connected to one of said sensed data generation circuits (fig. 3., col. 5 lines 30-44.)

Re claim 4, Hou discloses all of the limitations of claim 4 (see the 102(e) rejection to claim 3 supra), including wherein said sensed data generation circuit includes a latch circuit for latching a count value after the conversion operation start point of said counter upon reception of an output from the voltage-time conversion circuit of each group-selected pixel (fig. 3A indicator 314-n, col. 6 lines 45-51.)

Re claim 11, Hou discloses all of the limitations of claim 11 (see the 102(b) rejection to claim 3 supra), including wherein said sensed data generation circuit includes a counter for counting a clock signal (fig. 3A indicator 311), and a latch circuit for latching a count value of said counter after a point offset from the conversion operation start point upon reception of an output from said voltage-time conversion circuit of each group-selected pixel (fig. 3A indicator 314-n, col. 7 line 17 – col. 8 line 15.)

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Simoni et al. (A Digital Camera for Machine Vision"; employing Applicant's disclosure of this prior art as provided in relation to Figure 12 of Specification) in view of Hou (US 6,587,145.)**

Re claim 17, Simoni, employing Applicant's disclosure of this prior art as provided in relation to Figure 12 of Specification, discloses a data conversion/output apparatus including a column decoder for selecting at once a plurality of pixels aligned on an arbitrary column from pixels arrayed in a matrix (fig. 12 indicator 72), a plurality of data buses each commonly connected to a plurality of pixels aligned on each row out of the pixels (fig. 12 indicator 74), a counter for sequentially outputting count values in accordance with internal count operation (fig. 12 indicator 76), a plurality of latch circuits which are arranged on respective rows and latch the count values from said counter in accordance with level changes of said data buses corresponding to the respective rows (fig. 12 indicator 77), a row decoder for selecting a row having a desired pixel out of the pixels selected by said column decoder (fig. 12 indicator 73), and a plurality of row switches which are arranged on the respective rows and output as sensed data of desired pixels the count values latched by said latch circuits corresponding to the respective rows (fig. 12 indicator 75), wherein each of the pixels has a sensor for outputting a detection result as an output voltage value (fig. 12 indicator 73), and a column switch for outputting in accordance with selection of a pixel by said row decoder



an output to a data bus connected to the pixel (Specification – fig. 12 indicator 63.)

However, Simoni does not disclose a voltage-time conversion circuit for changing an output level upon the lapse of time corresponding to an output voltage value from said sensor after a predetermined conversion operation start point and further does not disclose a counter for sequentially outputting count values in accordance with internal count operation and for operating independently of the matrix, and a maximum value of the counter is arbitrarily adjustable.

Nevertheless, Hou discloses a data conversion/output apparatus that includes a voltage-time conversion circuit that changes an output level upon the lapse of time corresponding to an output voltage value from said sensor after a predetermined conversion operation start point (col. 3 line 4 col. 4 line 52). Additionally, Hou discloses sensed data generation circuits (fig. 3, 314-1 – 314-n) that include a counter (311) for sequentially outputting count values in accordance with an internal count operation (320) (col. 6, lines 45-58). The clock signal (320) is applied at mark time signal connector (310) from which the counter (311) counts the time marks in the clock signal (320) (col. 6, lines 47-50). Additionally, Hou states that the counter 311 continues counting of time marks and is reset only at the end of light integration (col. 6, lines 62-65). Thus, it can be seen that the counter operates independently of a pixel array, and a maximum value of the counter is arbitrarily adjustable (the counter 311 maximum value depends on the length of light integration). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the voltage-time conversion circuit and the counter of the data conversion/output apparatus as taught by

Hou with the data conversion/output apparatus as taught by Simoni, in order to produce signals of higher fidelity, as well as to accomplish A/D conversion within a pixel without requiring each pixel to have the extra circuitry and costs associated with conventional A/D circuits ('030 – col. 1 lines 33-62.)

Re claim 18, Simoni and Hou disclose all of the limitations of claim 17 (see the 103(a) rejection to claim 17 supra), including disclosing a data conversion/output apparatus further comprising a plurality of output-side latch circuits which are interposed between said latch circuits and said row switches for the respective rows, latch outputs from said latch circuits in accordance with a predetermined data reception signal, and output the outputs to said switches (Figure 12 of Specification, indicator 77.)

### ***Contacts***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on **(571) 272-7372**. The fax phone number for submitting all Official communications is **(571) 273-7300**. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at (571) 273-7312.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLJ



LIN YE  
SUPERVISORY PATENT EXAMINER